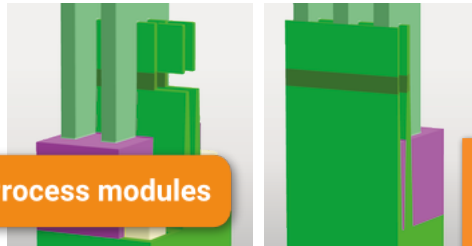


## Process Emulation for Your needs

- Process flow design
- Variability & yield
- DTCO

### MDI Module

#### 2 Process modules



#### Dummy Gate Etch

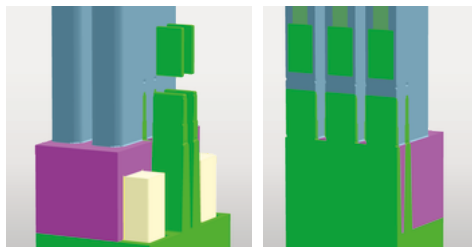


#### 3 Process steps

#### SiGe Removal & Gate Spacer Depo



#### Top Fin Etch & Cover Spacer Depo



#### Bottom Fin Recess

MDI formation process module for a next-gen CFET. Investigating the impact of vertical insulation on subsequent process steps as well as final device performance during optimization within the DTCO flow.

#### 1 Layout

GDSII

#### Technology templates

- CMOS devices
- 3D NAND flash
- DRAM
- Emerging devices

#### 4 Device

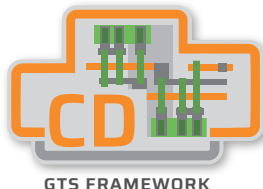
#### 5 Electrical characteristics

PEX

Get ready for new technologies – design the best process flow for your next-generation FET. Use flexible process modules to easily explore new designs. Study variability and optimize for device PPA as well as production yield.

### Your Benefits

- Flexibly change and combine process modules
- Investigate the impact of each process step
- Full interoperability with process simulation
- Reliability & variability comprehensively covered
- Robust and computationally efficient
- Full integration with TCAD and DTCO



# GTS CELL DESIGNER + PROEMU

## DTCO with the process in mind



### Process-Aware DTCO

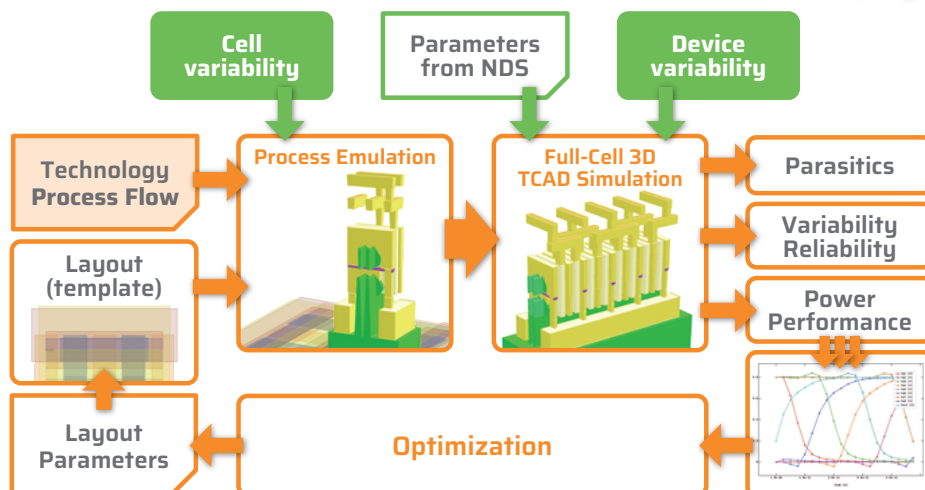
GTS ProEmu conveniently brings the process to DTCO – a perfect match with GTS CellDesigner:

Understand how each process step affects device performance. Tune your technology, leap ahead.

Explore key technology parameters with design and process in mind:

- Variability in masks & processes
- Identify critical process steps
- Examine effects down the line
- Study the impact on reliability

Technologies differ increasingly. Optimize your process to get the most out of your FinFET, NSFET, NWFET, CFET designs.



Use your mask layouts and customize easy-to-use technology process flows to investigate single devices, cells, and circuits. Add process variation in your flow and understand critical process steps and their impact on power, performance, variability, and reliability. Use predictive device simulations (NDS), TCAD calculations, and spice in unison, to optimize your process, design, and technology.



GLOBAL TCAD SOLUTIONS

**Global TCAD Solutions GmbH** (GTS) was founded in 2008 as a research-driven European TCAD creator and supplier.

With its staff of active scientists (150+ publications) and highly experienced software engineers, GTS maintains a leading role in TCAD innovation. GTS' company mission is to make the latest scientific research available for industrial use: Via GTS products and via consulting and research projects, taking an active role in collaborations with academic as well as industry partners.

GTS provides powerful solutions based on models well-founded in physics, assisting clients to create and optimize outstanding devices and designs.



### GTS Product Portfolio

**GTS Cell Designer (CD)** allows various approaches to design-technology co-optimization (DTCO): Create simulation-ready 3D logic cell models solely based on layout & technology information, or emulate the process. Quickly screen technology options, analyze device/circuit-level implications of your design choices, process variations, variability (LER, RDD, mask misalign, etc.)

**GTS Nano Device Simulator (NDS)** is based on the direct solution of the sub-band Boltzmann transport equation (SBTE) including detailed scattering and tunneling models. These predictive physical models allow to explore and exploit device physics at the nano scale, such as crystal orientation, strain, and material composition. Get a well-optimized device design even before going to silicon – reducing both cost and time to market.

**GTS Framework** is a full 2D/3D TCAD suite including outstanding classical and quantum-mechanical device / circuit simulators, tools for reliability and variability analysis as well as a powerful job server for grid computing – all in a consistent, easy-to-use 3-level (graphical/tree/text-file) interface.

