

1.82

-0.602

DTCO as it works for You:

- SPICE as accurate as TCAD
- Variability and Reliability included

As variability is increasing with downscaling, it becomes vital for assessing new technologies. Our reliability- and variability-aware DTCO flow combines the accuracy of TCAD and the speed of SPICE simulations to create meaningful results, which allow to compare designs and technologies.



Example: Performance and Variability-Aware SRAM Design for Gate-All-Around Nanosheets



Both single FET and full SRAM structures are generated. The latter is only used for fast parasitics-extraction (PEX) to obtain the full SRAM netlist, while FETs are extensively characterized with TCAD to extract accurate BSIM-CMG model cards, including variability. Combining the SRAM netlist with the FET model cards allows fast SPICE simulations.





Your Benefits

- A DTCO flow that actually works
- Accuracy of TCAD (using GTS' physical models)
- Speed & flexibility of SPICE
- Valid data across technologies
- Reliability & variability included

For more, see our publications (IRPS, SISPAD 2021 and later), and visit globaltcad.com

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Predictions based on physics.

Excellent match of SPICE to full-cell TCAD



GTS CELL DESIGNER + LSG

Optimize designs across technologies – without getting lost in the process

Pre-Silicon DTCO

Be ahead of the curve – optimize your designs before silicon data is available.

Focus on your application and explore key technology parameters:

- Power, performance, area
- Parasitics, thermal robustness
- Reliability, time-to-failure
- Variability, process variations

Deciding on a technology has big implications from device and cell to circuit and system level. With GTS Cell Designer (CD) you can benchmark technology options (FinFET, NWFET, NSFET, CFET, ...) and get the best design for each one of them.



Global TCAD Solutions GmbH (GTS) was founded in 2008 as a research-driven European TCAD creator and supplier.

With its staff of active scientists (150+ publications) and highly experienced software engineers, GTS maintains a leading role in TCAD innovation. GTS' company mission is to make the latest scientific research available for industrial use: Via GTS products and via consulting and research projects, taking an active role in collaborations with academic as well as industry partners.

GTS provides powerful solutions based on models well-founded in physics, assisting clients to create and optimize outstanding devices and designs.

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From the layout and technology description, a complete standard cell is created and simulated in a TCAD tool, accounting for variability on cell and device level. Physical transport parameters are extracted from predictive device simulations (NDS). TCAD calculations yield all relevant metrics (power / performance / variability / reliability) for the standard cell and intrinsically consider all coupling effects (parasitics). The design team uses this information to optimize the layout.

GTS Product Portfolio



GTS Cell Designer (CD) allows various approaches to design-technology cooptimization (DTCO): Create simulation-ready 3D logic cell models solely based on layout & technology information, or emulate the process. Quickly screen technology options, analyze device/circuit-level implications of your design choices, process variations, variability (LER, RDD, mask misalign, etc.)



GTS Nano Device Simulator (NDS) is based on the direct solution of the sub-band Boltzmann transport equation (SBTE) including detailed scattering and tunneling models. These predictive physical models allow to explore and exploit device physics at the nano scale, such as crystal orientation, strain, and material composition. Get a well-optimized device design even before going to silicon – reducing both cost and time to market.



GTS Framework is a full 2D/3D TCAD suite including outstanding classical and quantum-mechanical device / circuit simulators, tools for reliability and variability analysis as well as a powerful job server for grid computing – all in a consistent, easy-to-use 3-level (graphical/tree/text-file) interface.



