



A Decade of Driving Innovation
Physics-based DTCO • Full-Cell 3D TCAD



Predictions based on physics.

Today's semiconductor industry is facing unprecedented challenges.

To survive in highly competitive markets such as high-performance logic and memory, strategic leadership is mandatory.

*One of the key instruments to staying successful in this business is **predictive simulation in technology CAD (TCAD)**.*

Traditional simulation software has stopped being predictive for the past several nodes already – a new paradigm is needed.

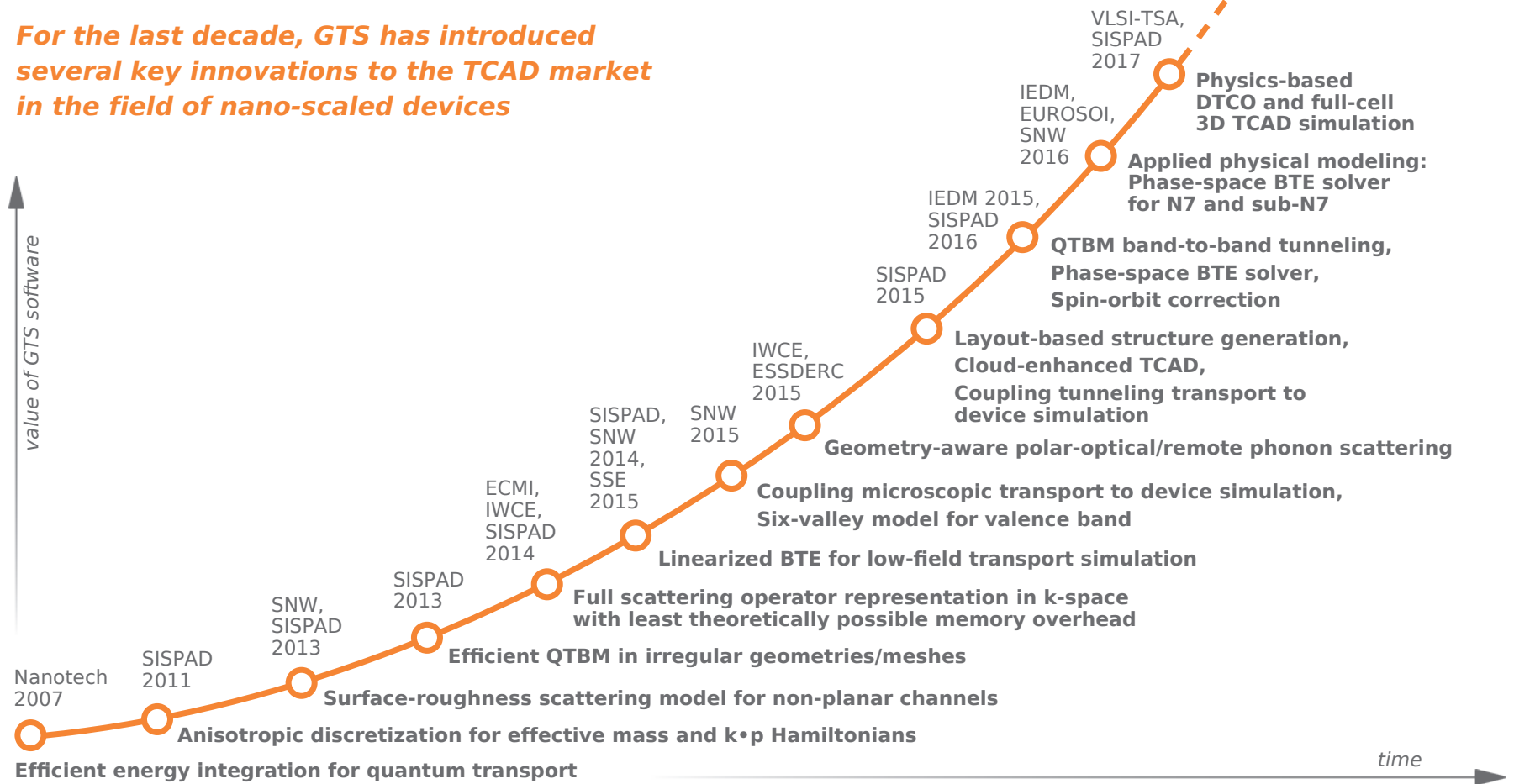
*Global TCAD Solutions has been pushing development of this new paradigm, which we call **physical device modeling**.*

Physical device modeling is the only solid base for nano-scale TCAD.

Leading the Way to Nano TCAD



For the last decade, GTS has introduced several key innovations to the TCAD market in the field of nano-scaled devices



GTS – The Leading Specialists in Physical Device Simulation, Since 2007

Introducing a New Paradigm

At the core of GTS' predictive physical models lies a **long tradition of scientific research**. GTS staff have contributed to the state of the art of physical device modeling in **more than 150 scientific publications** (at SISPAD, SNW, ECS, ULIS, EURO-SOI, IWCE, ESSDERC, DRC, IEDM, IEEE Electron Device Letters, Solid State Electronics, Journal of Computational Electronics, etc.). This expertise has helped GTS to create simulation tools that cover all the important physical aspects of modern, nano-scale devices, such as:

- Quantum confinement
- Full band structure
- Non-equilibrium Boltzmann transport
- Carrier scattering
- Quantum tunneling

Equally focused on **industrial** application, GTS has developed a rich, modular TCAD framework to include all effects into a single simulation flow, accompanied by a consistent user interface.

ESSDERC 2015
Predictive Physical Simulation of III/V Quantum-Well MISFETs for Logic Applications
Z. Stanojević*, O. Baumgartner, V. Essler, E. Mitterbauer, H. Demel, C. Kernstock*,
†Institu
Email: {z.stan

IEDM 2015
Physical Modeling – a New Paradigm in Device Simulation
Z. Stanojević, O. Baumgartner, V. Essler, E. Mitterbauer, H. Demel, C. Kernstock*,
†Institu
Email: {z.stan

SNW 2015
Bringing Physics to Device Design – a Fast and Predictive Device Simulation Framework
M. Karner, Z. Stanojević, O. Baumgartner, H. W. Karner, C. Kernstock, H. Demel, F. Mitterbauer
Global TCAD Solutions GmbH, Bösendorferstraße 1/12, 1010 Vienna, Austria
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SISPAD 2016
Phase-Space Solution of the Subband Boltzmann Transport Equation for Nano-Scale TCAD
Z. Stanojević, M. Karner, O. Baumgartner, HW. Karner, C. Kernstock, H. Demel, and F. Mitterbauer
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IEDM 2016
Vertically Stacked Sub-10 nm Nano-Devices with Tunable Variability
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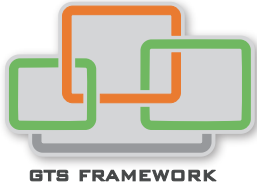
Abstract—We present a comprehensive simulation framework for transport modeling in nano-scaled devices based on the solution of the subband Boltzmann transport equation (BTE). The BTE is solved in phase space using a k-p-based electronic structure model and includes all relevant scattering processes. The BTE solver is combined with a conventional drift-diffusion-based simulator using a novel iteration approach. The pairing between BTE, DD, and Poisson results in a flexible toolkit which converges quickly in any mode of operation, allows large-scale parallelization, and to include near-equilibrium transport outside the BTE region, i.e. the contacting regions. The toolkit is commercially available as part of the GTS Nano Device Simulator (NDS). We examine realistic NMOS and PMOS devices, including the impact of the electrostatic scale and possible quantum



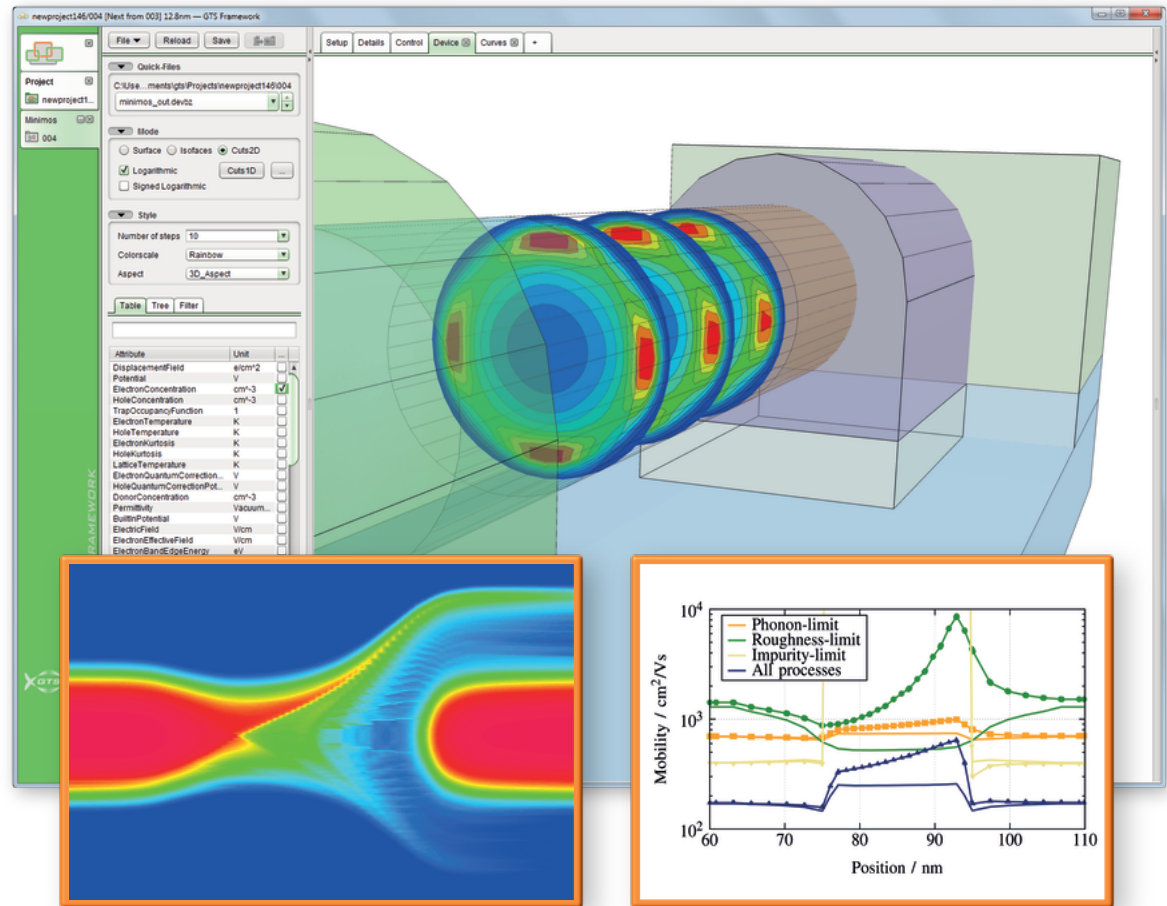
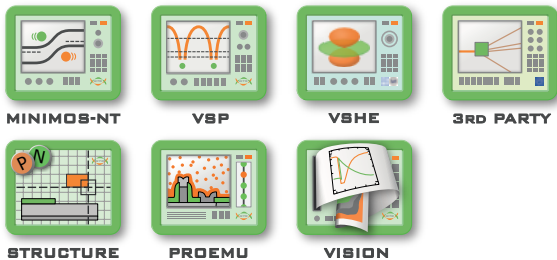
Creating the Tools for Today's Industry

A Solid Base: The Framework

A solid modern working environment is the infrastructure for creating powerful tools and implementing efficient workflows for our customers.



GTS Framework is home to classic and quantum-mechanical device, and circuit simulators, tools for structure generation and editing, visualization, optimization, DOE, file storage, distributed computing, and optionally also third-party tools.



Time-Zero Variability on Device and Cell Level, Integrated Circuit Simulation

RDD, MGG, LER, Discrete Traps

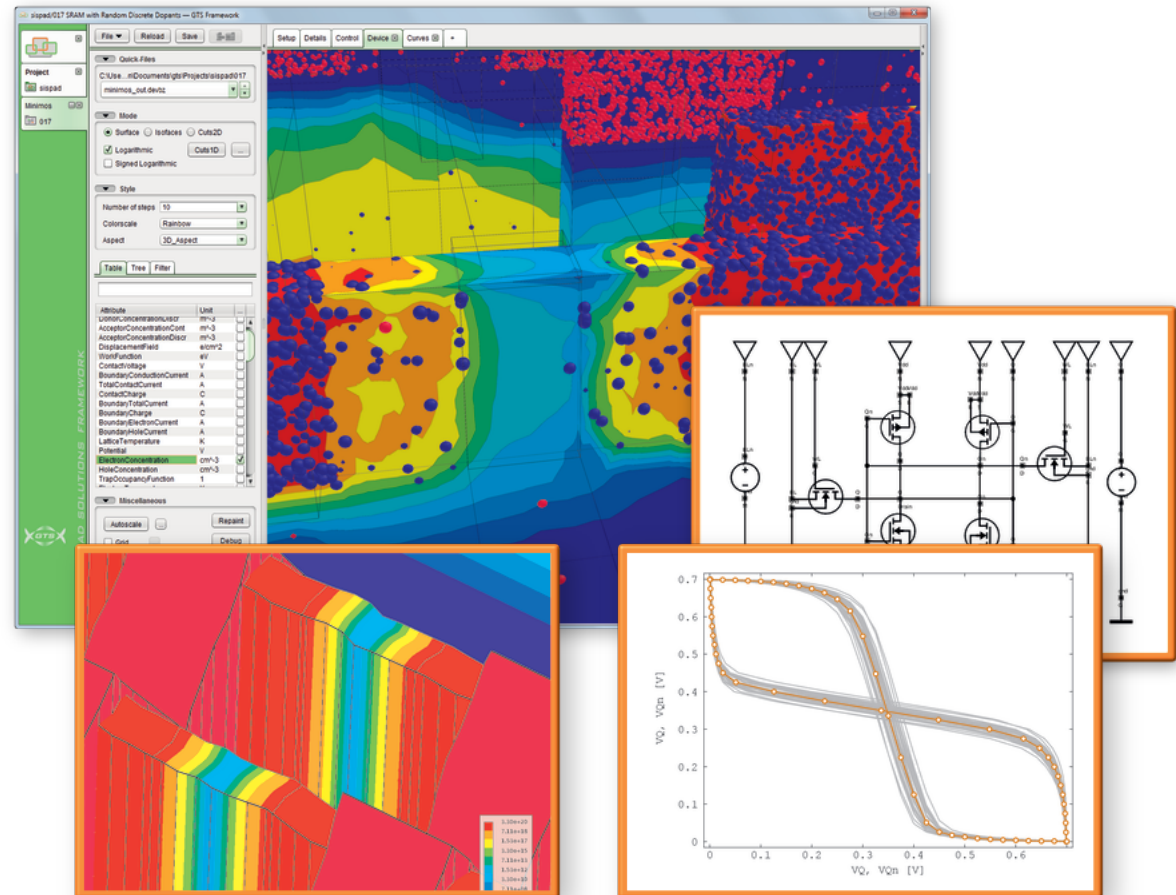
Since device feature size is approaching atomistic scales, self-averaging of device properties for individual devices becomes less effective and variability is becoming a major concern for CMOS scaling and integration. Careful analysis of intrinsic fluctuation on circuit and system level is vital to reduce variability and **increase yield**.

GTS Framework offers an accurate yet efficient model to predict and also "design" fluctuations in electrical device characteristics; the **built-in mixed-mode** allows analyzing impact on circuit level.

The Monte Carlo analysis can be performed with **full device simulation** or using the **impedance field method (IFM)**.

Dominant variability sources can be introduced automatically to the 3D device- and circuit simulation model, such as:

- Random discrete dopants (**RDD**)
- Line-edge roughness (**LER**), including various process-induced fluctuations
- Mask misalignment
- Metal grain granularity (**MGG**)
- Discrete oxide and interface traps



Optimizing Reliability by Knowing Degradation Physics

Managing Reliability

Profound understanding of the degradation physics is key to engineering reliability in your technology – for instance by reducing defect density, shifting traps in energy, or reducing the electrostatic impact.

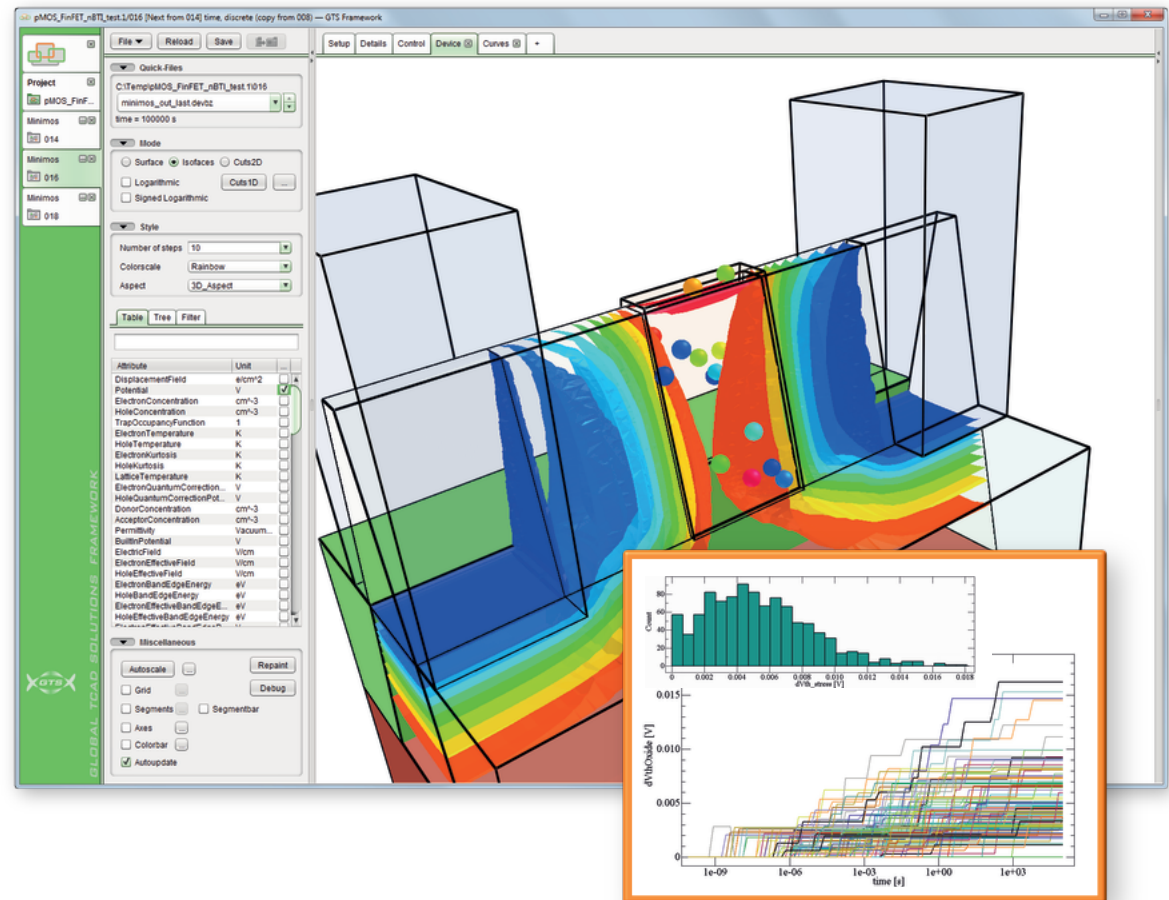
Non-ideal device behavior can be caused by defects at the semiconductor-insulator interface as well as inside the insulating oxide. One of the most critical degradation mechanisms in p-channel CMOS devices, **NBTI**, as well as other phenomena are **accurately modeled** in GTS Framework:

- Bias temperature instability (NBTI, PBTI) covered by non-radiative multi-phonon (NMP) and double-well (DW) model
- Hot-carrier degradation (HCI, HCD)
- Time-dependent dielectric breakdown
- Random telegraph noise (RTN)

Use inverse modeling where appropriate.

Radiation Effects

GTS Framework allows to study radiation effects such as single-event upset (**SEU**), single event transient (**SET**), and the total ionizing dose (**TID**).

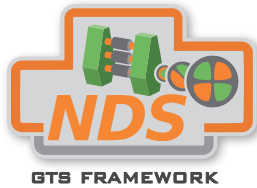




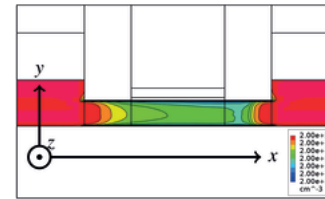
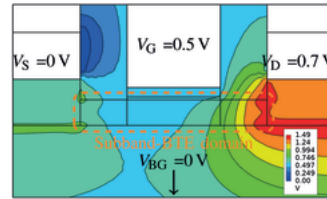
Physics Matters – GTS Nano Device Simulator

Why Physical Modeling?

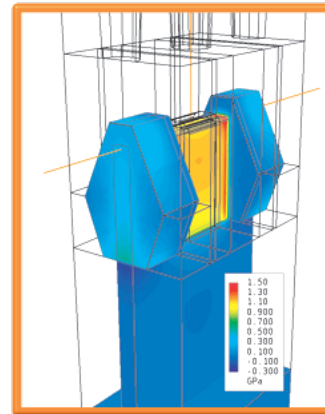
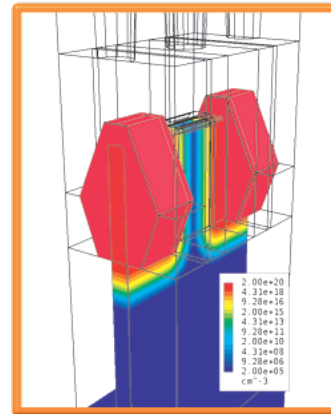
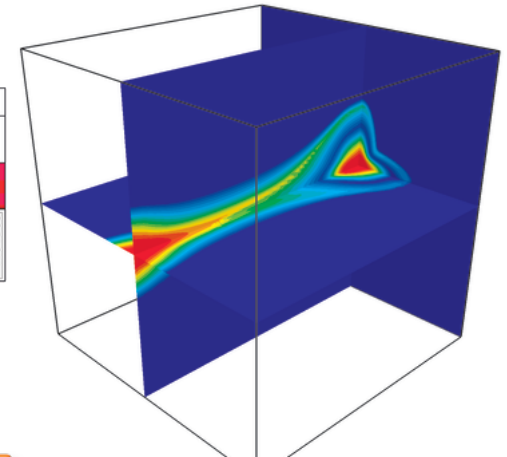
In nano-scaled devices, multiple scattering mechanisms apply. Thus, methods relying on relaxation time approximation yield spurious and incomplete results. For valid predictions, a new approach is needed.



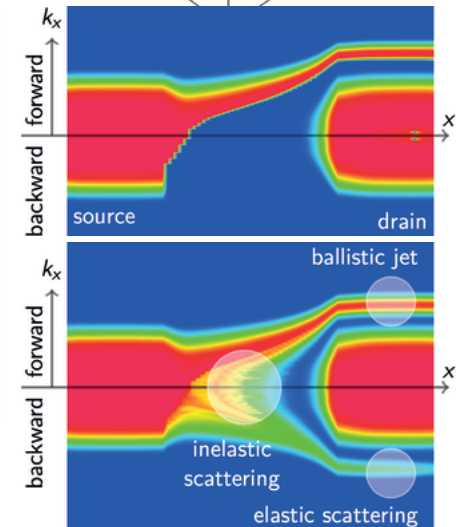
GTS **Nano Device Simulator** relies on the full solution of the Boltzmann transport equation (BTE) on sub-bands. Its predictive **physical models** allow to explore and exploit device physics at the nano scale, such as crystal **orientation**, **strain**, and **material composition**. You can create a **well-optimized device design** before going to silicon. This leads to shorter time to market and results in **enormous cost savings**. Reliability modules help assess **variability**, **device aging**, and **radiation effects** long before first fabrication.



NMOS FDSOI device: Potential and electron concentration. Right: Electron distribution function in 3D phase space.



NMOS FinFET: Doping profile and axial stress due to lattice mismatch between fin and strain-relaxed buffer (SRB). Right: Scattering mechanisms denoted in phase-space.



 **Path-Finding, Based on Valid Predictions by GTS Nano Device Simulator**

Profound and Valid Predictions

Next to the benefits of getting profound results, physical modeling keeps model parameters **portable**. This allows you to calibrate them using your existing mature technology nodes, and from there **cast reliable predictions** for the nodes under development – key for profound decisions in **path-finding** as well as **DTCO**.

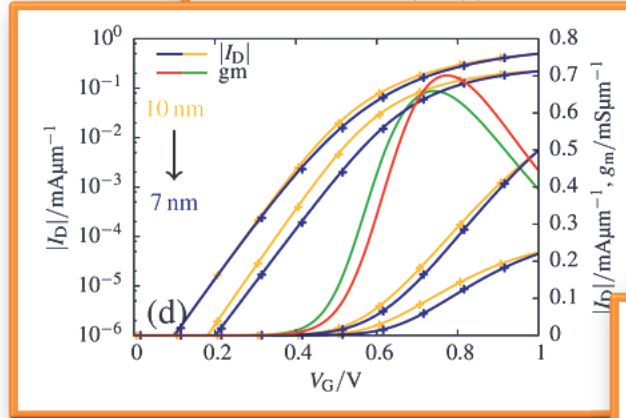
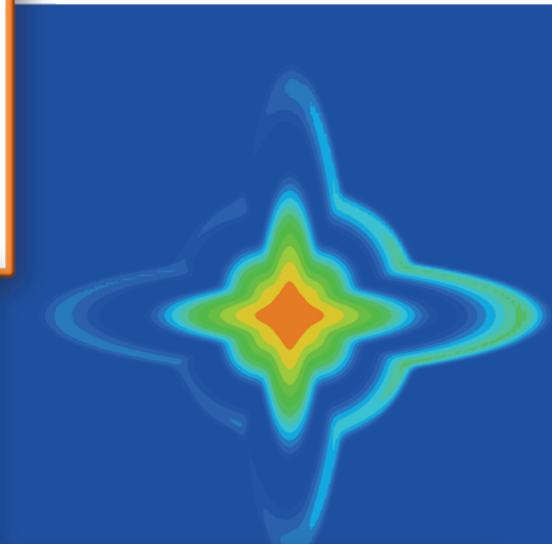
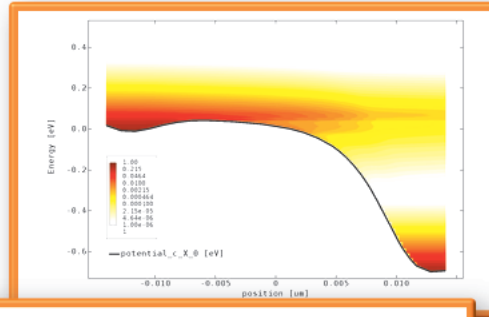
Physical modeling also allows to integrate results from **first-principles methods** into device simulation – which would not be possible using traditional tools.

Solid Data Format

Real-world structures are rarely strictly rectangular. Describing boundary surfaces without compromise is fundamental for obtaining accurate results in such highly delicate calculations.

GTS models make use of **unstructured meshes in 2D as well as 3D** to achieve full accuracy and lossless interoperability with industry-standard tools.

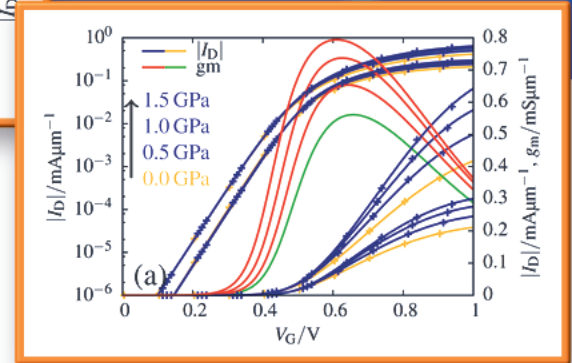
Top left: Band edge profile along NMOS FinFET device with electron distribution in color.



Top right: Hole distribution in k-space near the drain of an FDSOI PMOS.

Bottom left: FDSOI NMOS gate length scaling: Transfer characteristics and off-current for 10 nm and 7 nm, respectively.

Bottom right: FDSOI NMOS I_{ON} enhancement by uni-axial tensile stress.



From Path-Finding to Cell Simulation – Automated Parameter Fitting

From Accurate to Fast

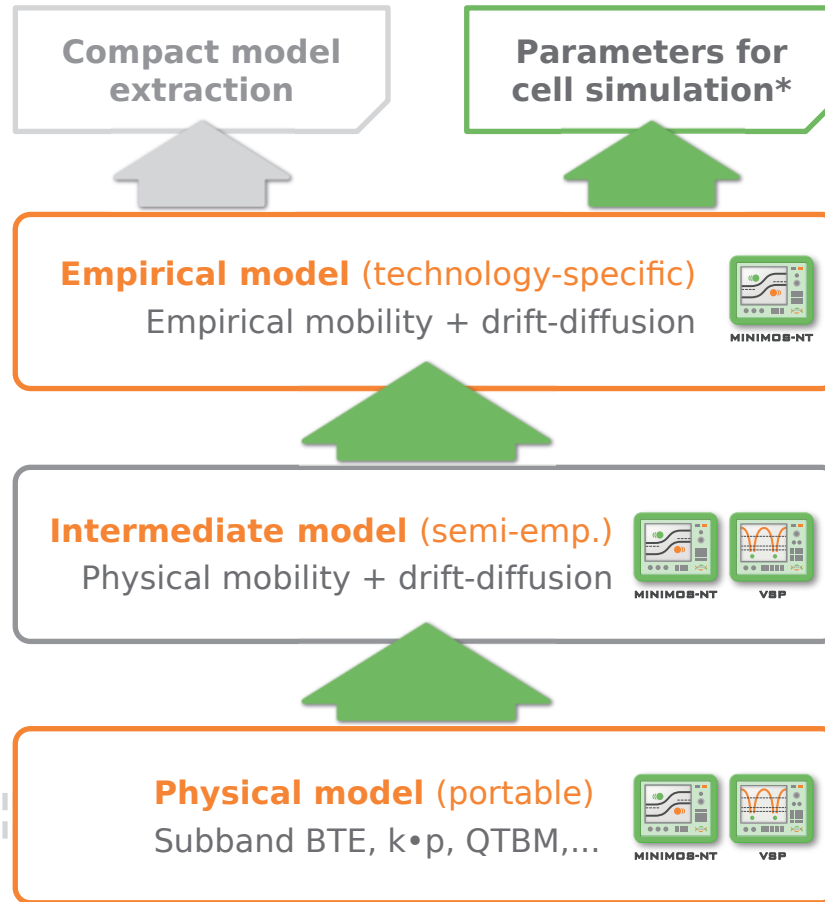
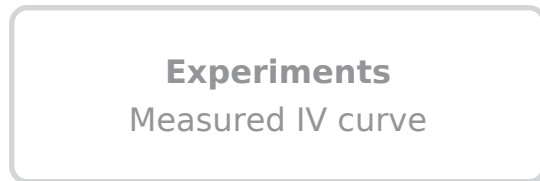
Our physical models run amazingly fast. Once they are calibrated, you want to efficiently shift gears towards performing full-cell 3D simulations with much faster empirical models.

At each stage you can select which parts of carrier transport to model physically and which ones empirically. The intermediate assists the calibration process by separating the low-field, high-field, and ballistic components of transport modeling.

The resulting parameters are ready to use for cell simulation – see page 12.

Results You Can Rely On

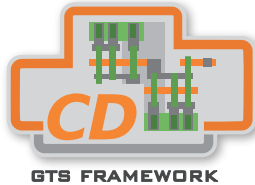
GTS Framework is available with its models fitted to the imec technology FinFET nodes N14, N10, N7, and NWFET node N7.



Rapid Creation of Simulation-Ready Cells

Layout-based Structure Generation

Combining process emulators with device simulators poses difficulties, ranging from technical ones such as artifacts and large mesh sizes to organizational ones such as limited access to detailed process data. We have a much faster, yet valid alternative.

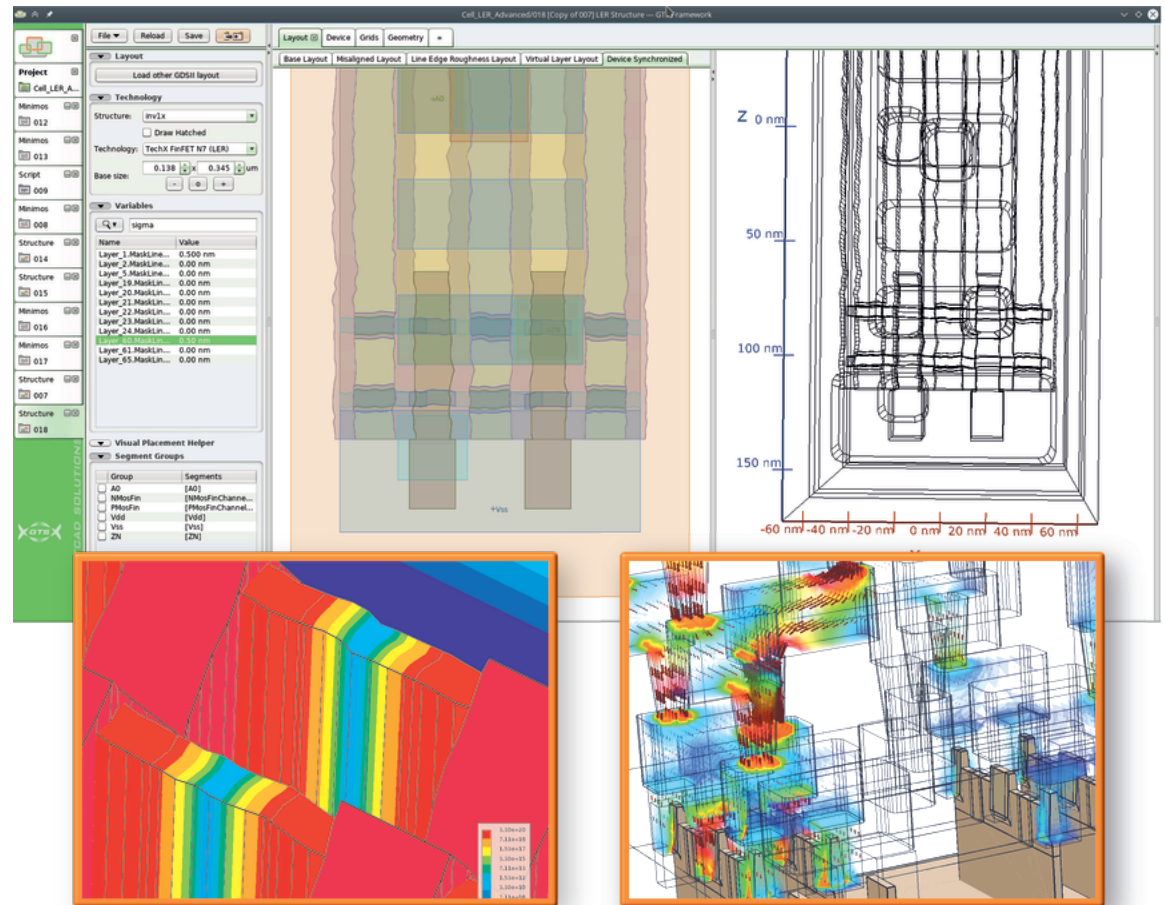


The LSG within GTS **Cell Designer** creates **simulation-ready** full-cell structures based on layout files and technology descriptions, which allows to efficiently analyze all circuit-level implications of:

- LER in fins, gates and BEOL
- Mask misalignment
- Lithography effects

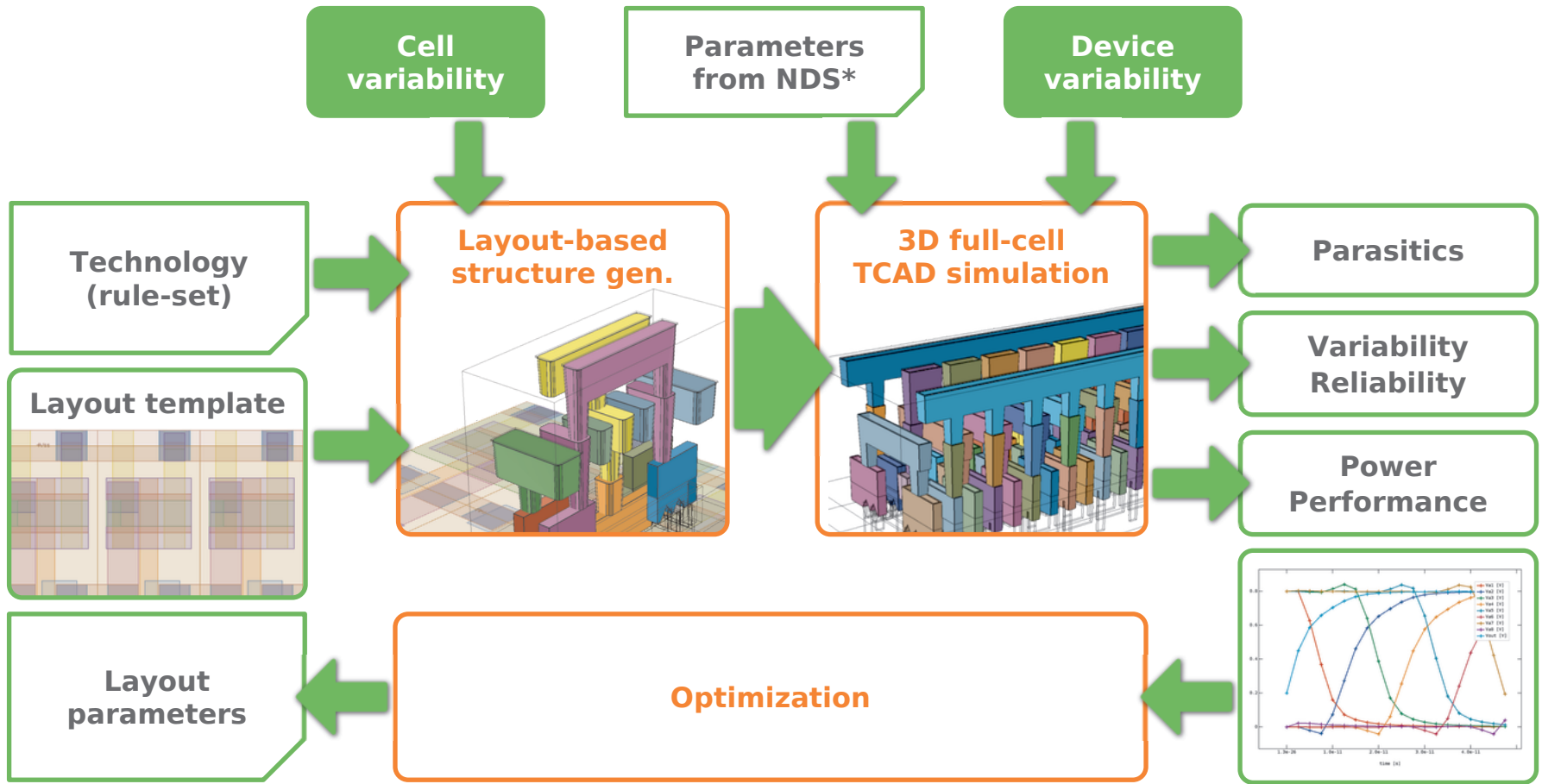
Features:

- Device-to-device correlation
- Combined FEOL / BEOL modeling
- Awareness of self-alignment techniques

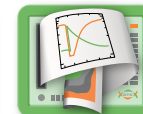
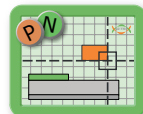
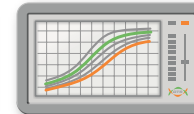
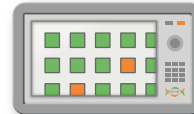
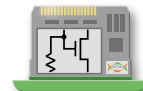
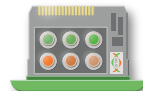
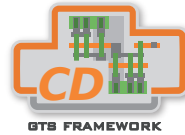
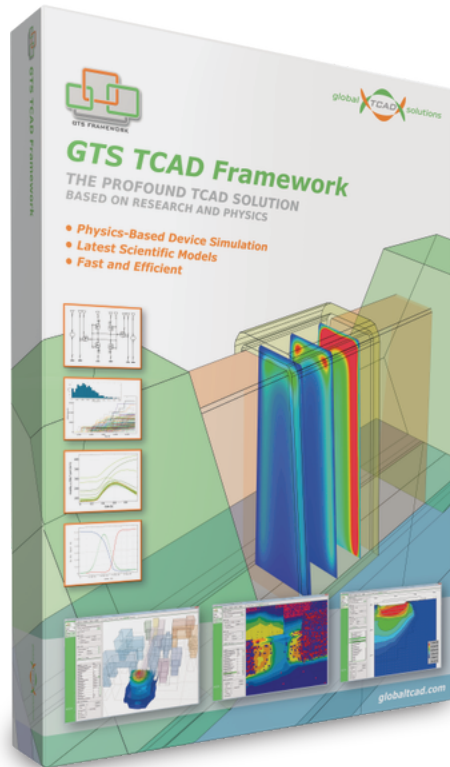




GTS Cell Designer - The DTCO Workflow that Works



GTS Framework – A Comprehensive Set of Outstanding TCAD Tools



Strong Partnerships

GTS relies on in-house scientific expertise as well as **cooperations** with world-class scientists and organizations such as TU Wien, imec, and ST-Microelectronics.

First-Hand Support

GTS provides **consulting** as well as **first-hand product support** to clients, aiming to help creating outstanding products and to solve any issues quickly and thoroughly.

Company & Perspectives

Global TCAD Solutions GmbH (GTS) was founded in 2008 as a spin-off company from Vienna University of Technology (TU Wien).

With its staff of proficient scientists as well as experienced software developers, and collaborations with renowned research organizations, GTS is determined to maintain its leading position in TCAD innovation for years to come.

GTS' perspective is to make latest scientific research rapidly available for industrial use, creating the most revolutionary, comprehensive, and efficient yet easy-to-use nano TCAD that money can buy.



Zlatan Stanojević, CTO

A former scientist at the Institute for Microelectronics at TU Wien, Zlatan joined Global TCAD Solutions to become its CTO. As an expert in electronic structure and transport calculation in nano-electronic devices as well as in fast numerical methods, Zlatan is also chief developer of the VSP quantum simulator.



Markus Karner, CEO

Markus Karner studied electrical engineering at TU Wien, where he worked for European and national projects since 2004. His personal interests include modeling and simulation of quantum effects in nano-scaled CMOS technology. As co-founder and CEO of GTS, he is in charge of project management and business development.

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