**Self-Heating Aware Logic Cell Design and Optimization**

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**Self-Heating 3D TCAD Simulation of Complete Logic Cell**

- **Layout**: GDSII file
- **Technology**: Description file (ITF-like)
- **Layout-based Structure Generation (LSG)**:
  - FEOL (fins with tapered buffers, rounded edges, anisotropic epi blocks)
  - BEOL (contacts, interconn.)
- **3D TCAD Model Device Simulation**:
  - Full-cell TCAD simulation
  - Including self-heating
- **R/C Extraction**:
  - Calculate thermal R/C
  - Extract electric parasitics
- **PPA, Reliability, Temperature**:
  - Analyze thermal cell properties, compare designs & technologies

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**Incorporating Self-Heating in Cell Design • TCAD DTCO**

**Reasoning**
- Smaller devices, interactions within cells increase
- Augmenting TCAD-based DTCO (design and technology co-optimization) with thermal awareness is becoming obligatory in cell design

**SH Simulation: Time-Scale Issue**
- Average dissipated power of one cycle
- Calculate temperature due to dissipated power
- Verified on 2D MOS full transient thermal profile
- Capturing the long-term thermal behavior by simulating only one transient cycle

**Thermal Resistance by Technology**

- **FinFET**
- **Nanosheet**
- **Nanowire**
- **CFET**

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**Results: Technology Comparison**

- Average heat generation during one full inverter cycle.
- Input for fast temperature profile calculation with various thermal boundary conditions.

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**Your Benefit**

- Identify local thermal hot spots
- at device/cell/block level
- depending on load and layout
- for each specific cell technology
GTS CELL DESIGNER

Optimize designs across technologies – without getting lost in the process

Pre-Silicon DTCO

Be ahead of the curve – optimize your designs before silicon data is available.

Focus on your application and explore key technology parameters:
• Power, performance, area
• Parasitics, thermal robustness
• Reliability, time-to-failure
• Variability, process variations

Deciding on a technology has big implications from device and cell to circuit and system level. With GTS Cell Designer (CD) you can benchmark technology options (FinFET, NWFT, NSFT, CFET, ...) and get the best design for each one of them.

GTS Product Portfolio

GTS Cell Designer (CD) takes a practical approach to design-technology co-optimization (DTCO): Create simulation-ready 3D logic cell models based on layout and technology information. Quickly screen technology options and analyze device and circuit-level implications of your design choices, process variations, and variability (LER, RDD, mask misalignment, ...).

GTS Nano Device Simulator (NDS) is based on the direct solution of the subband Boltzmann transport equation (SBTE) including detailed scattering and tunneling models. These predictive physical models allow to explore and exploit device physics at the nano scale, such as crystal orientation, strain, and material composition. Get a well-optimized device design even before going to silicon – reducing both cost and time to market.

GTS Framework is a full 2D / 3D TCAD suite including outstanding classical and quantum-mechanical device / circuit simulators, tools for reliability and variability analysis as well as a powerful job server for grid computing – all in a consistent easy-to-use graphical interface.

Global TCAD Solutions GmbH (GTS)

Global TCAD Solutions GmbH (GTS) was founded in 2008 as a spin-off from Vienna University of Technology (TU Wien).

With its staff of active scientists (150+ publications) as well as experienced software engineers, GTS maintains a leading role in TCAD innovation. GTS' company mission is to make the latest scientific research available for industrial use – in GTS products as well as in consulting and research collaborations with academic and industry partners.

GTS provides powerful solutions based on models well-founded in physics, assisting clients to create and optimize outstanding devices and designs.

Predictions based on physics.